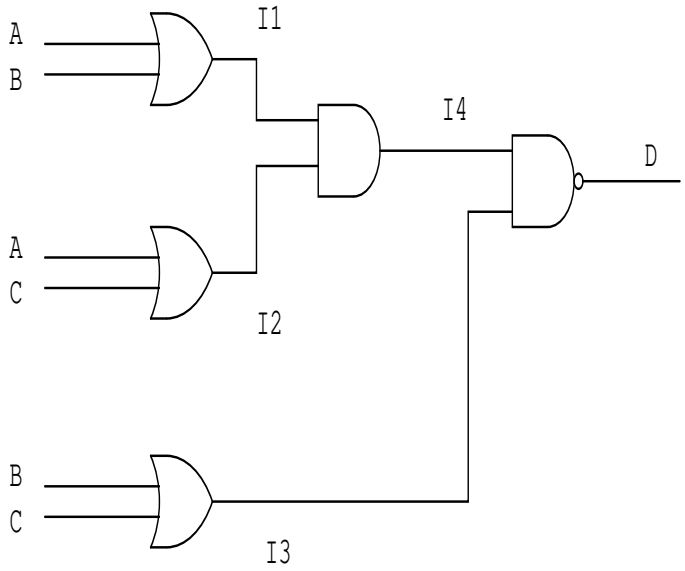
Experiment 1

With reference to the combinational system specified in the following logic schematic:



Task (T1): Perform symbolic analysis.

Deliverable (D1): Network expression specifying `D` in terms of `A`, `B` and `C`.

Task (T2): Perform literal analysis.

Deliverable (D2): Truth table with one output column for each of `I1, I2, I3, I4` and `D`.

Task (T3): Develop a structural Verilog model of the combinational system using the Verilog models for the TTL ICs SN7432, SN7408 and SN7400.

Deliverable (D3): Electronic submission of source code (`make submit`).

Task (T4): Map your Verilog model to a TTL-based physical design for the combinational system.

Deliverable (D4): IC logic schematic.

Task (T5): Specify IC interconnections.

Deliverable (D5): One completed pin-out sheet (at least) for each IC employed in your physical design.

Task (T6): In the laboratory, wire-up your physical design, verify its behaviour and sign-off on the design/implementation.

Deliverable (D6): A physical realization of the combinational system that behaves to specification. Details of the circuit-verification process. Student signature indicating that the circuit behaves as specified.

Task (T7): Document any relevant results, explanations or comments.

Deliverable (D7): A section in your report entitled Results/Explanations/Comments in which you have detailed any relevant results, explanations or comments.

NOTES