Digital Logic and Computer Organization

Sequential Logic —Flip Flops

Problems with Gated Latches

- Gated latches are still not well suited for synchronous sequential systems because the potential of multiple state changes in one clock cycle.

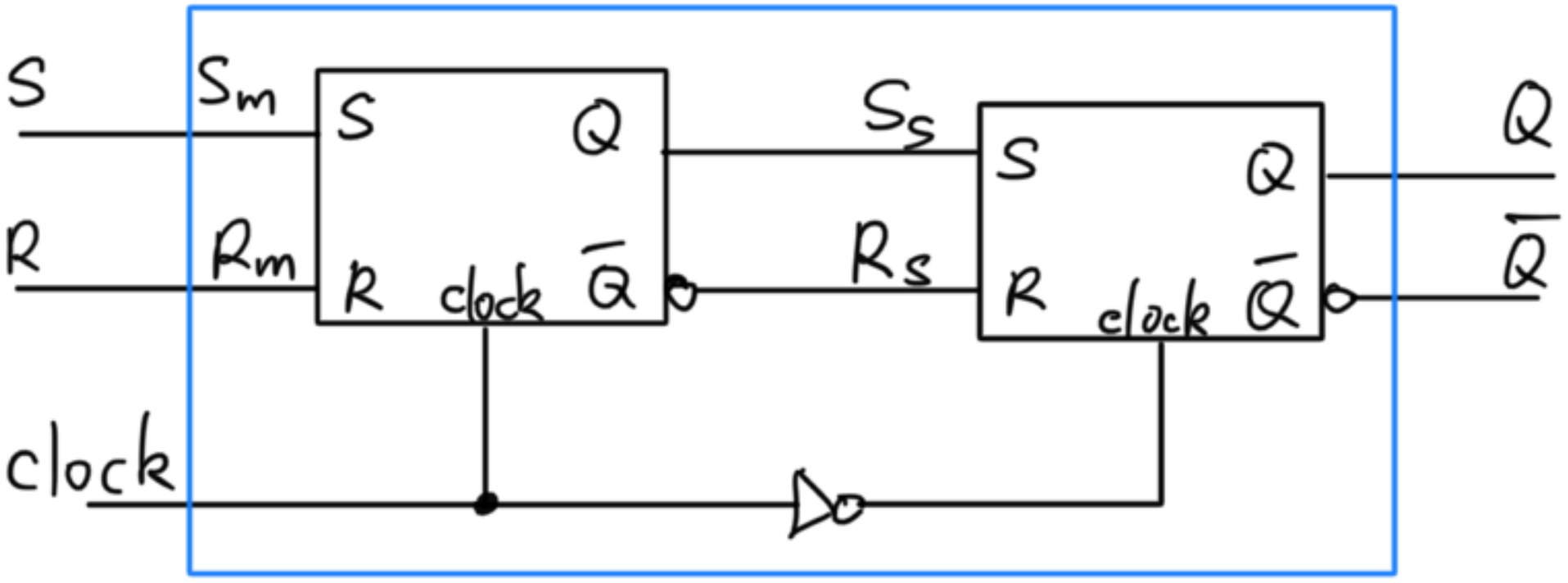
- How to fix it?

  - use a master-slave configuration

  - shorten clock pulse so that there is only one state change per clock cycle (not likely)

  - use edge triggered flip flops

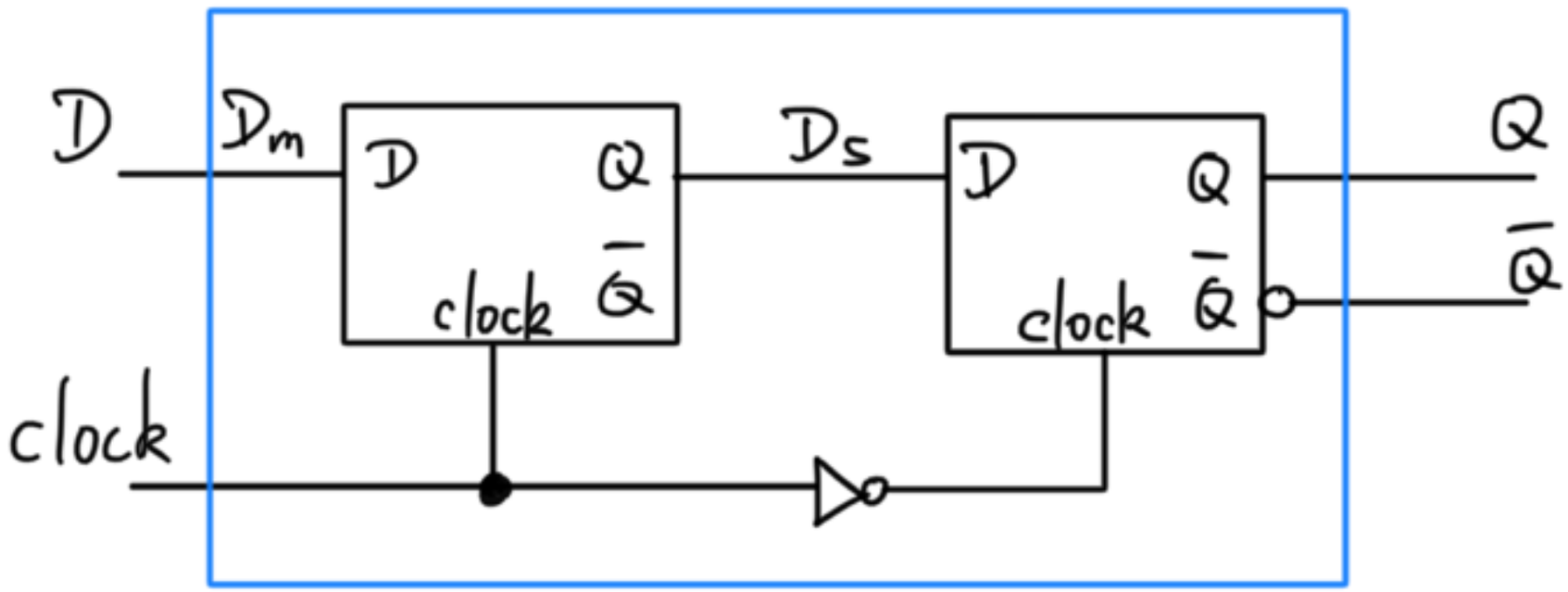
Negative Master-Slave SR Flip Flops



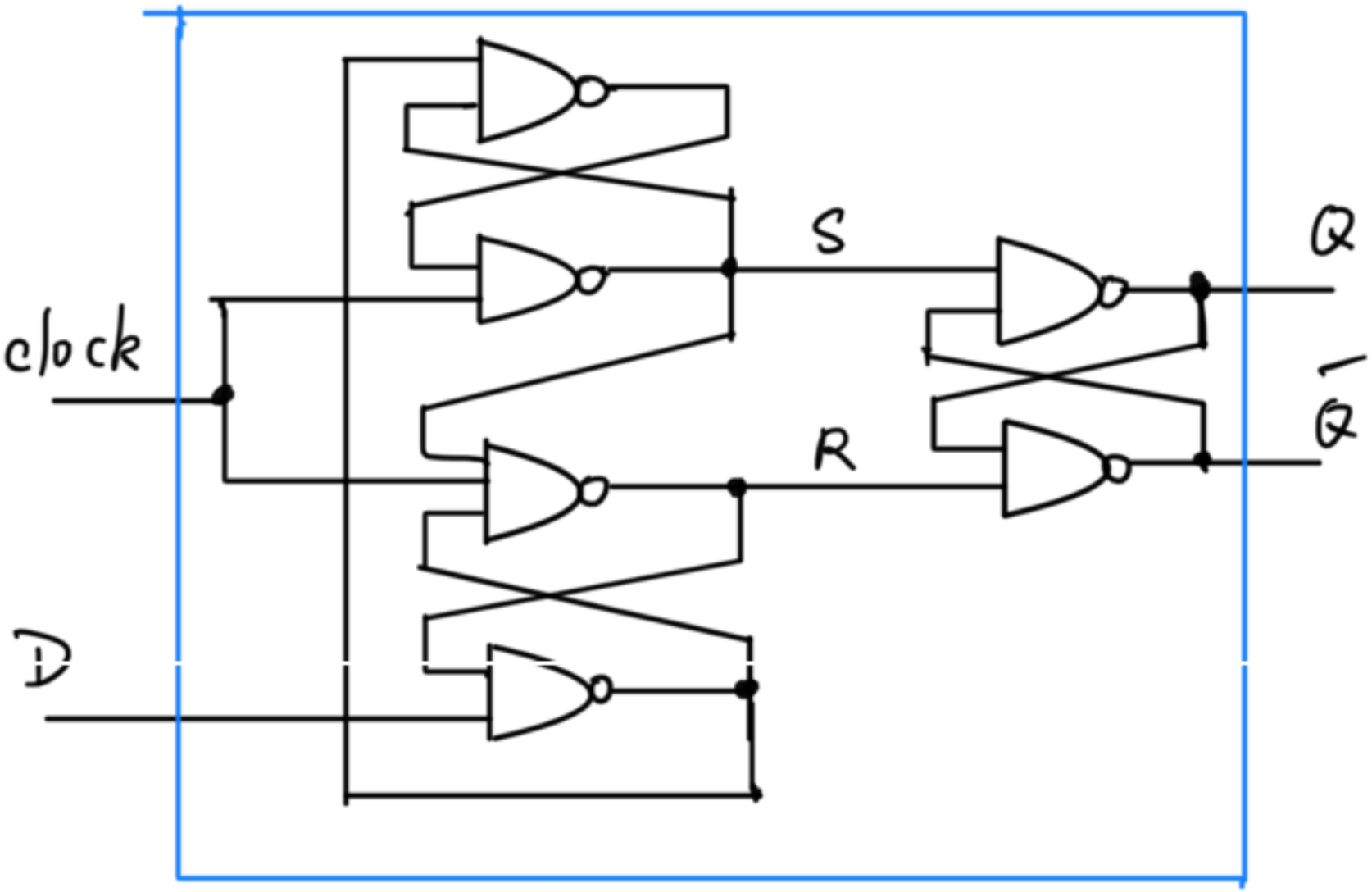
Problem

- The previous device is pulse triggered
- When the master is enabled, a glitch can incorrectly set/reset the master output, which is also the slave input
- Fix: move to edge-triggered devices
  - Positive edge triggered: outputs are generated on the rising edge
  - Negative edge triggered: outputs are generated on the falling edge

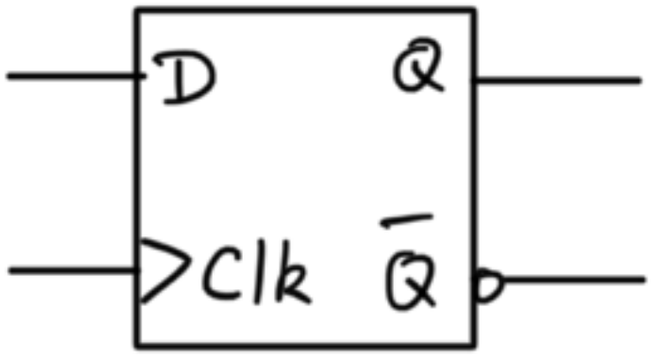
Negative Edge Triggered Master-Slave Realization D Flip Flop

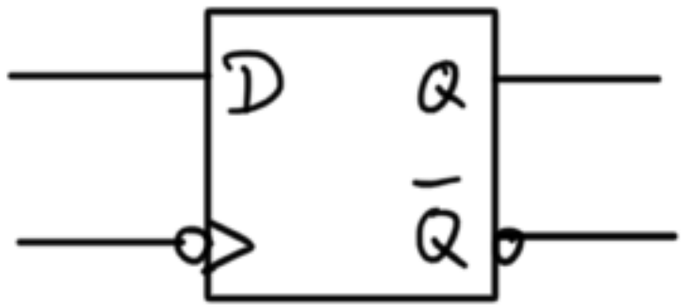


Positive Edge Triggered
Alternative Realization
D Flip Flop



Edge Triggered D Flip Flop Symbols

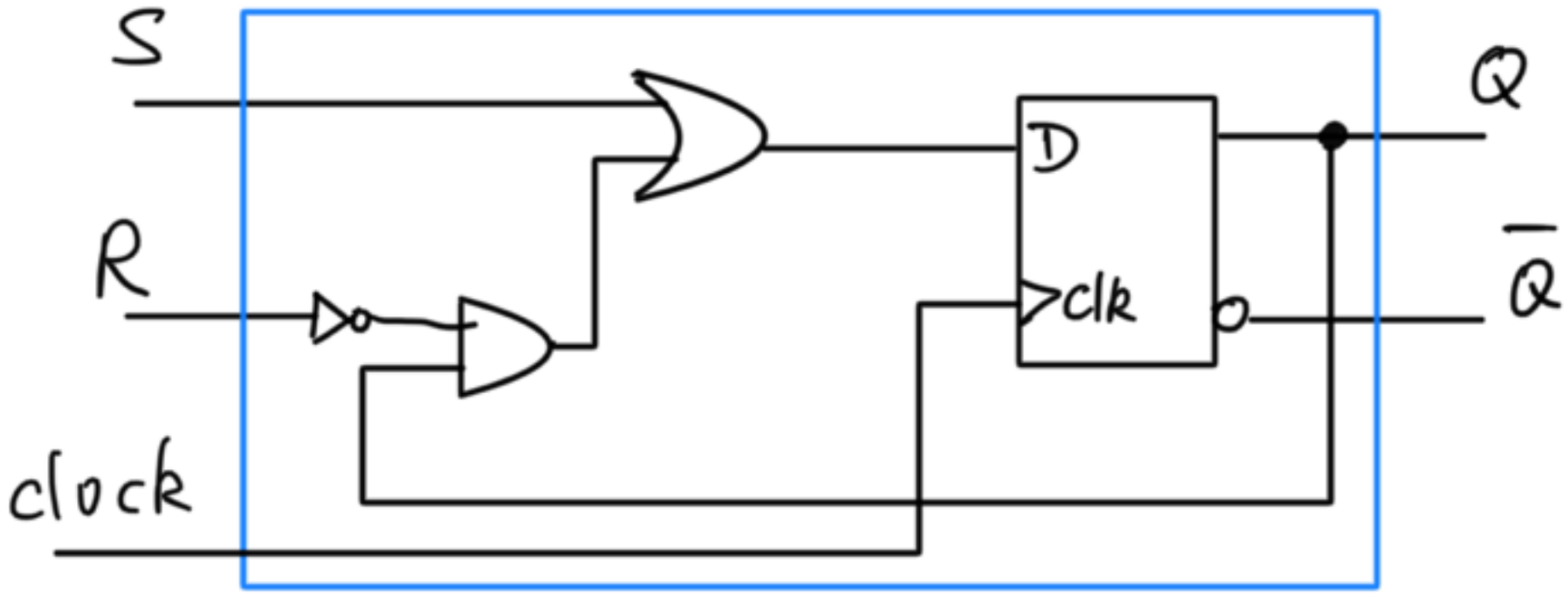




Excitation Table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

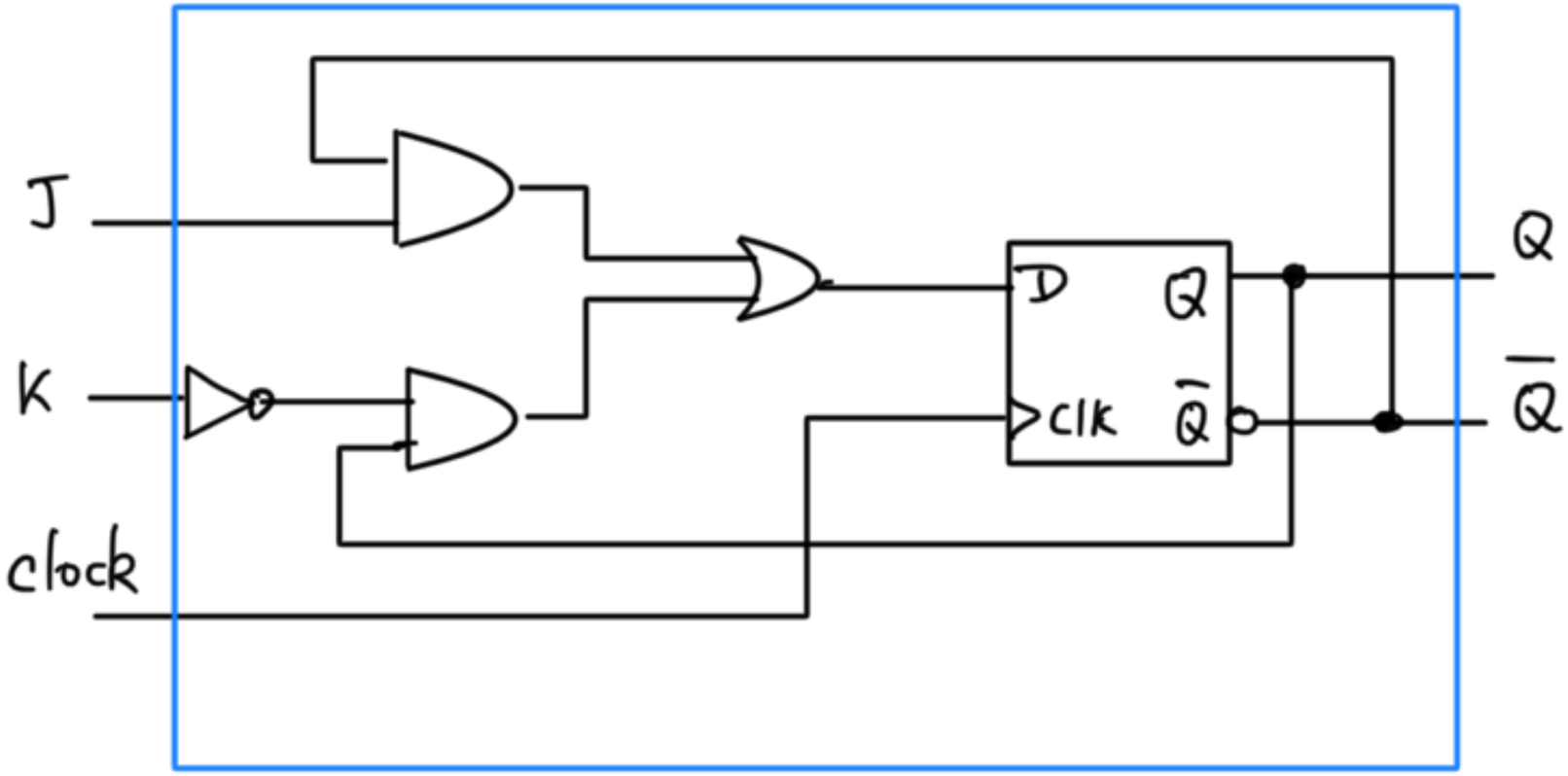
Edge Triggered SR Flip Flop



Excitation Table

Q	Q^+	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

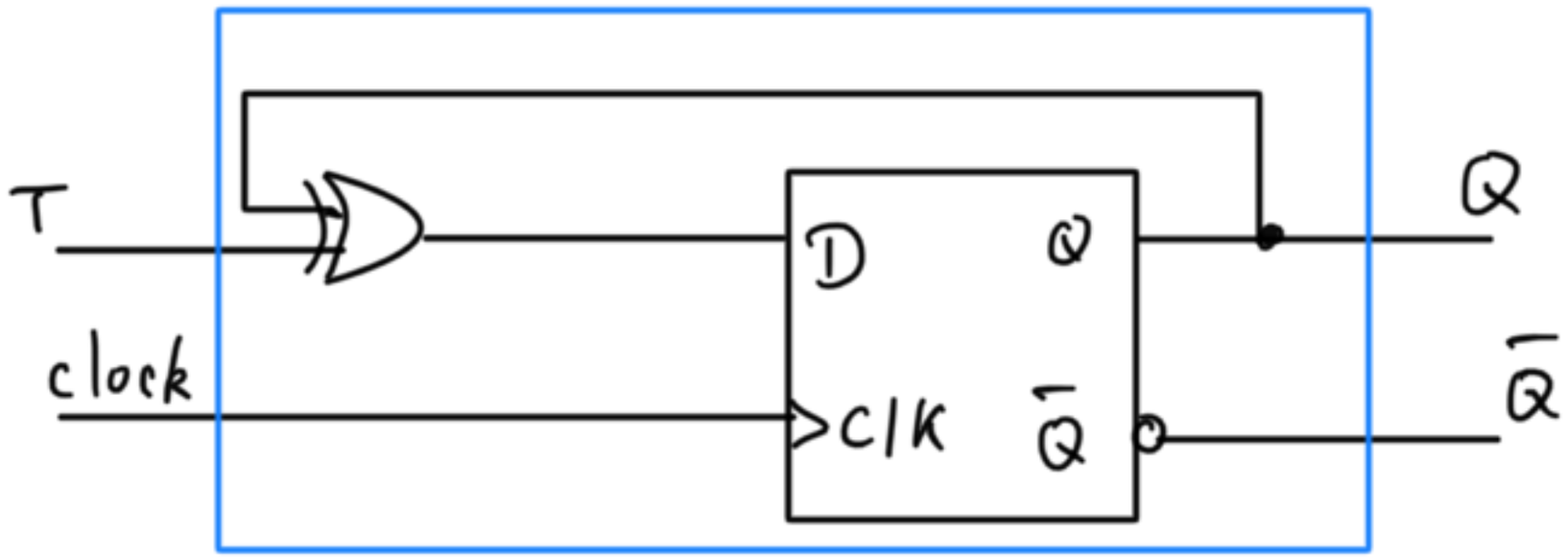
Edge Triggered JK Flip Flop



Excitation Table

Q	Q^+	J	k
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

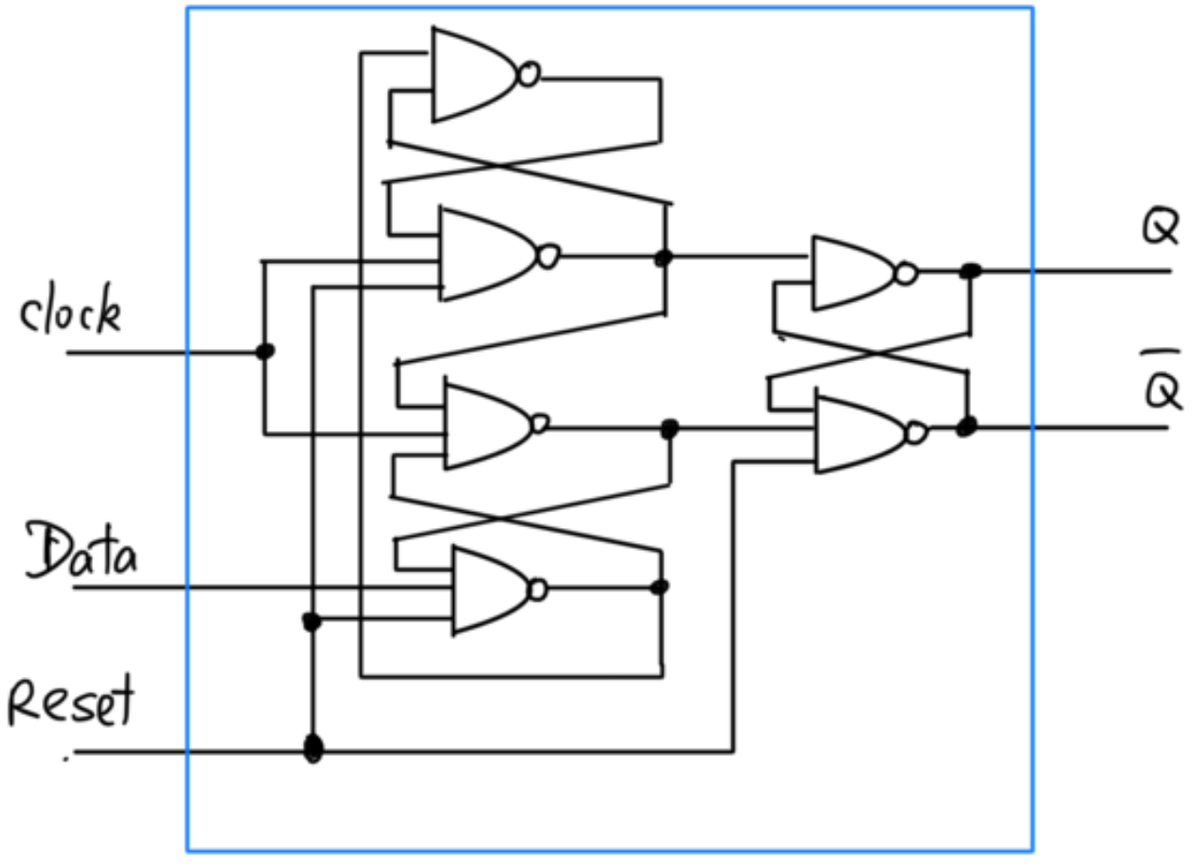
Edge Triggered T Flip Flop

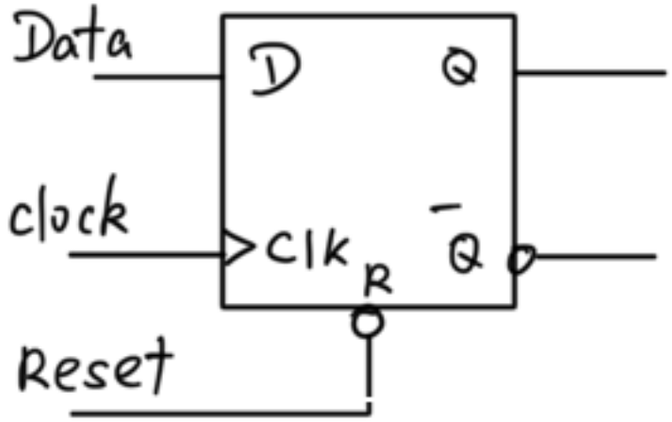


Excitation Table

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Edge Triggered D Flip Flop with Asynchronous Reset





Reset	Clock	Data	Q	$\overline{Q}$
0	x	x	0	1
1	↑	0	0	1
1	↑	1	1	0